CAVITY SIMULATOR FOR THE EUROPEAN SPALLATION SOURCE

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ABSTRACT

The Cavity Simulator will reproduce the behavior of superconducting elliptical cavities and high power amplifiers (klystron/IoT) used in medium and high beta sections of the European Spallation Source linac. The device will simulate all RF and analog signals from a single set of cavity and amplifier. It will be used to test LLRF systems after installation in the ESS facility.

The device is based on a high performance FPGA connected to a set of precise data converters with a dedicated analog frontend. Down-conversion scheme is used to digitize the input RF signals and all output RF signals will be generated using vector modulators. For the FPGA a custom firmware will be prepared. It will perform digital signal processing, data acquisition and handle communication over the Ethernet network. A dedicated software running on external PC for remote control of the device will be provided.

In this contribution the conceptual design and the current status of the Cavity Simulator project will be presented.

HARDWARE

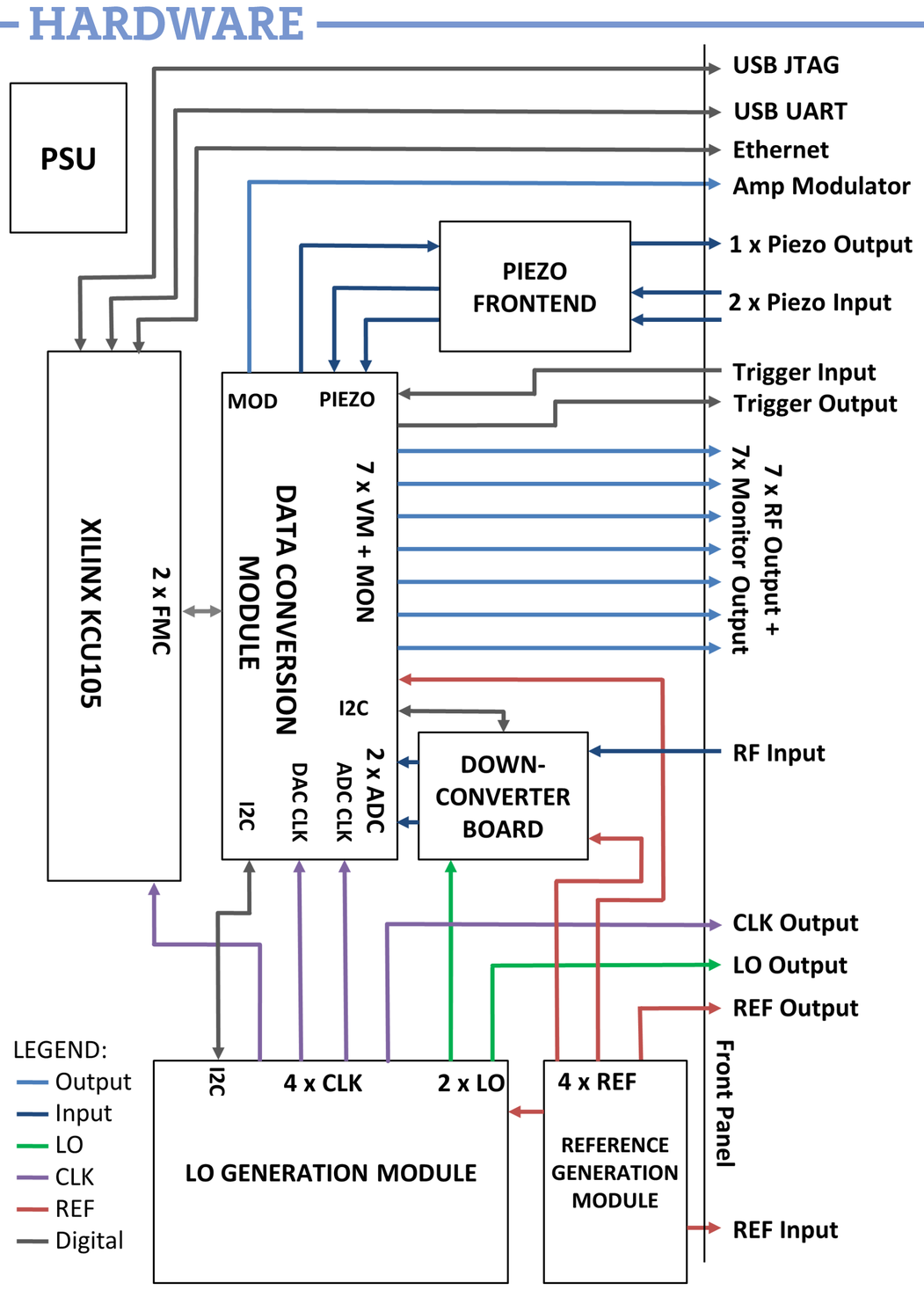

Figure 1: The block diagram of Cavity Simulator Hardware

ACKNOWLEDGMENT

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AMPLIFIER MODEL

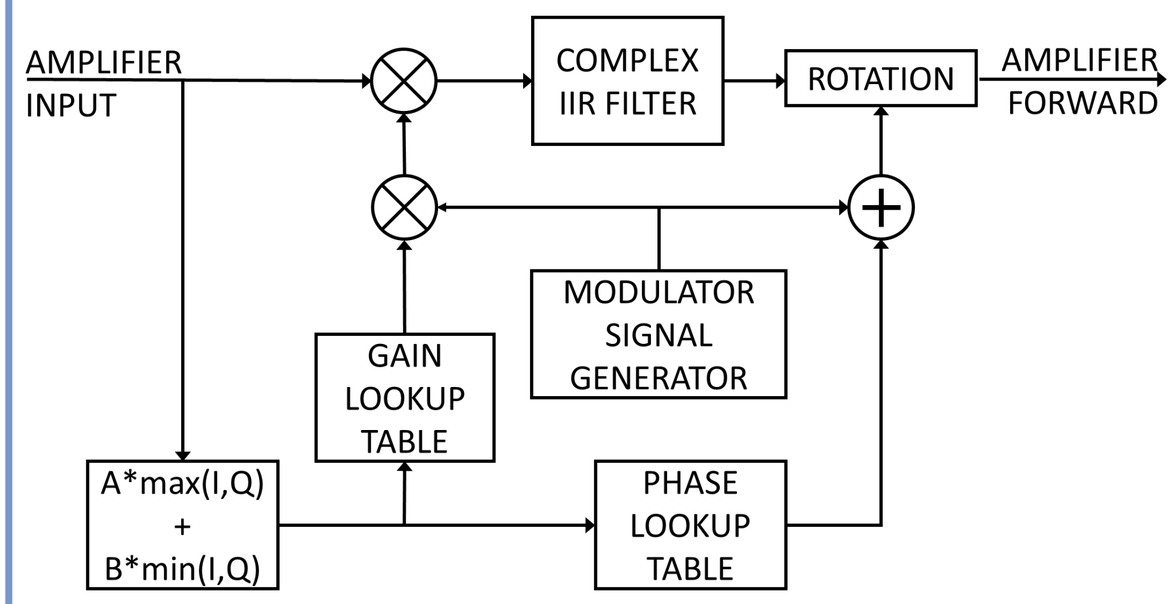

Figure 2: The block diagram of the amplifier model.

CIRCULATOR MODEL

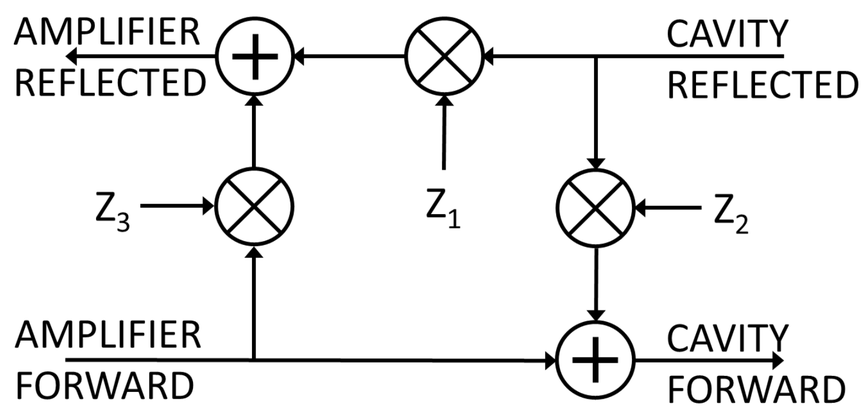

Figure 3: The block diagram of the circulator model.

CAVITY MODEL

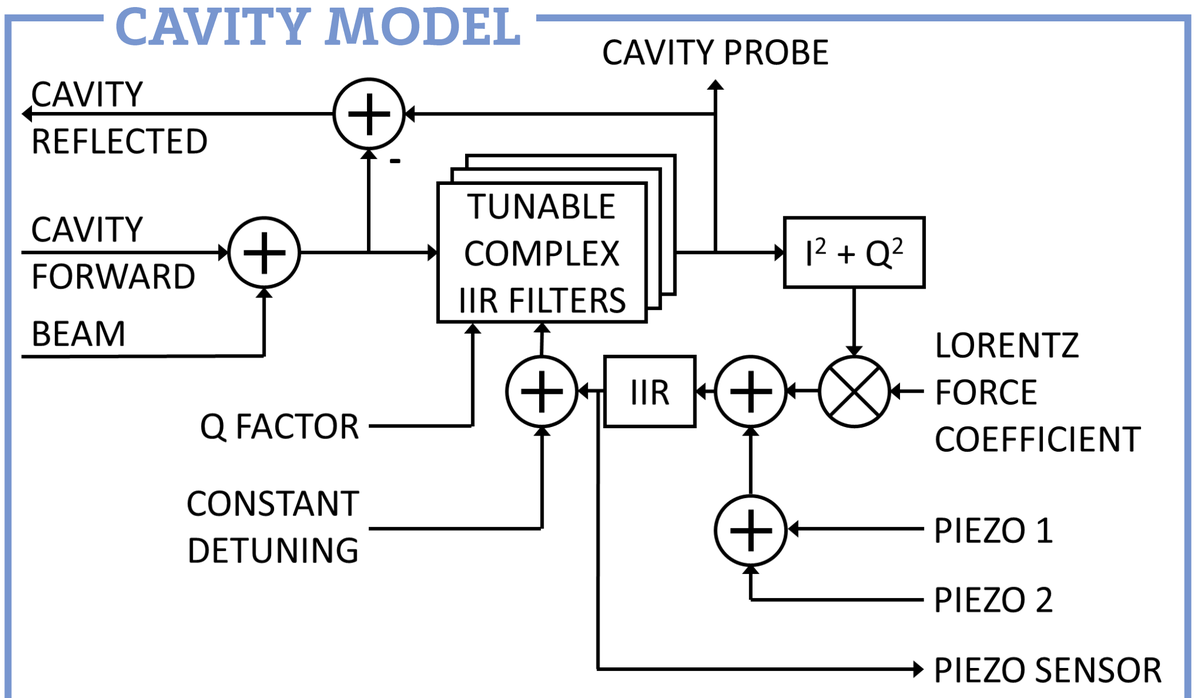

Figure 4: The block diagram of the cavity model

TUNABLE DIGITAL FILTER

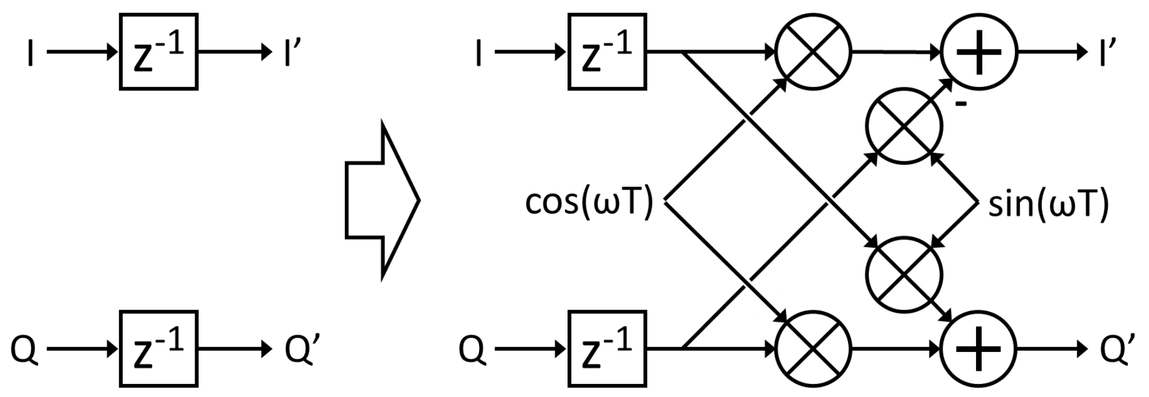

Figure 5: Modification of the filter delay block, that allows to shift the filter transmission.

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